PUE 3141: ADVANCED DIGITAL SYSTEMS DESIGN

LECTURE 1B

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Topics:

i) Review of sequential logic designs with flip flops (FF)

References:

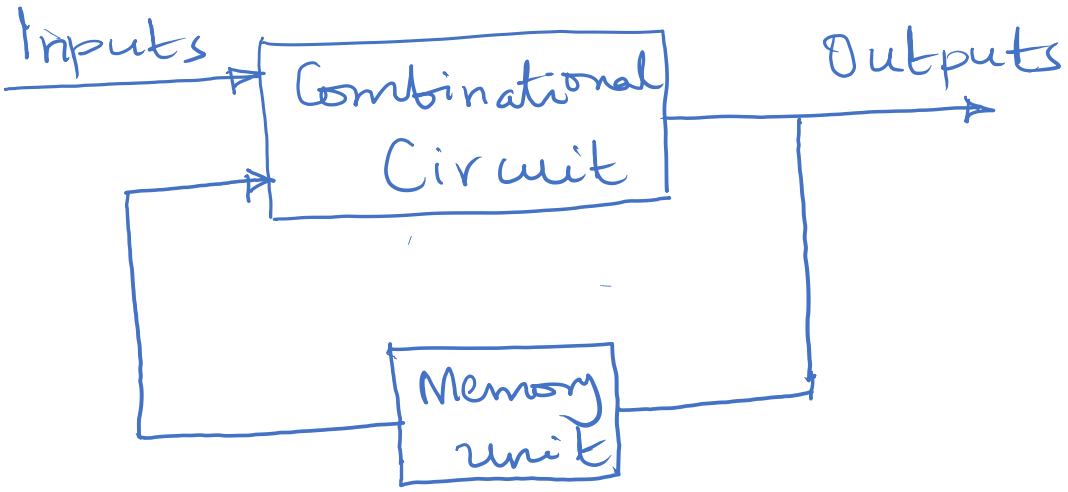
i) Elijah, M. (2009) *Foundations of Digital Electronics*. University of Nairobi Press

ii) Rafiquzzaman, M. (2005) *Fundamentals of Digital Logic & Microcomputer Design* (5th Edition). Wiley.

NB
* Examples to be provided in the physical class.

1. Review of Sequential Logic Designs with Flip Flops

Sequential logic circuit can be regarded as combinational circuit that incorporates memory as shown below:



Flip Flops

- This is the basic building block in the memory of electronic devices.
- It is a 1-bit memory unit with 2 stable states and is the basic memory unit in synchronous sequential logic systems.
- Common FFs include:

  i) SR Flip Flop ii) JK Flip Flop iv) D Flip Flop iii) T Flip Flop

- In sequential logic design using FFs, the following major steps are followed:

Characteristic Table & Equation → Excitation Table → State Diagram

Truth Table: What is the current output given a set of (current) inputs?

Characteristic Table: What is the next state, when we have a given set of inputs?

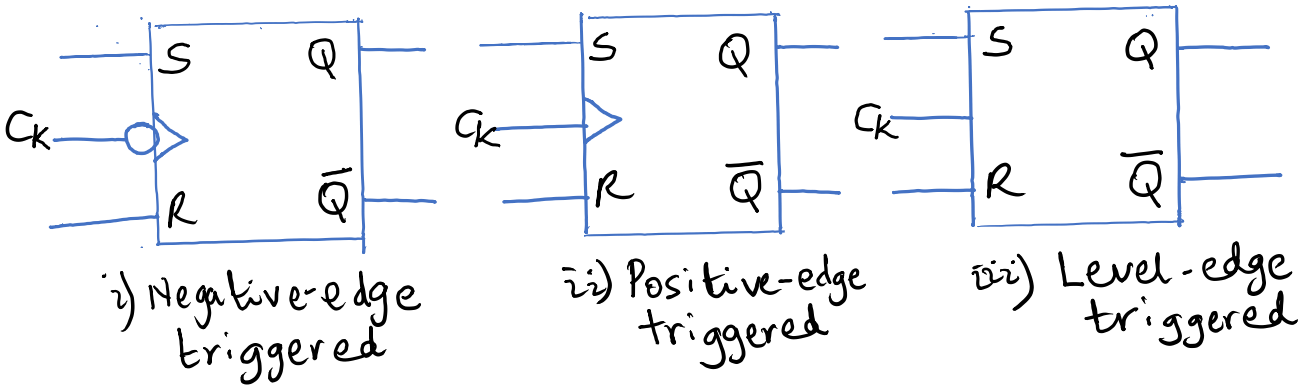
Excitation Table: We are in a certain present state and want a particular next state, what are the required inputs?

State Diagram: Transitions from one state to another and the input conditions necessary for the respective transitions.

Flip-flop Triggering

i) Negative-edge triggered: Output state changes on the falling edge of a clock pulse
ii) Positive-edge triggered: Output state changes on the rising edge of a clock pulse
iii) Level-triggered: Output changes during the time duration that the clock signal is at logic High (1) level.

The symbolic representation for the above 3 types of triggering are shown below. SR flip flop is used for the illustration:



A. SR (Set - Reset) Flip Flop

i) Characteristic Table of clocked SR FF

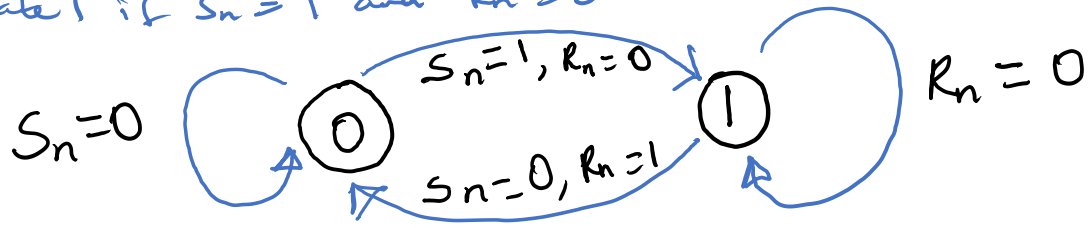
Inputs S_n	Inputs R_n	Next State Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

ii) Excitation Table of clocked SR FF

PS Q_n	NS Q_{n+1}	Required Inputs S_n	R_n
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

iii) State Diagram

The FF has 2 states : either $Q=0$ or $Q=1$. If it's in state 0, then after the application of a clock pulse it can make a transition to state 1 if $S_n=1$ and $R_n=0$



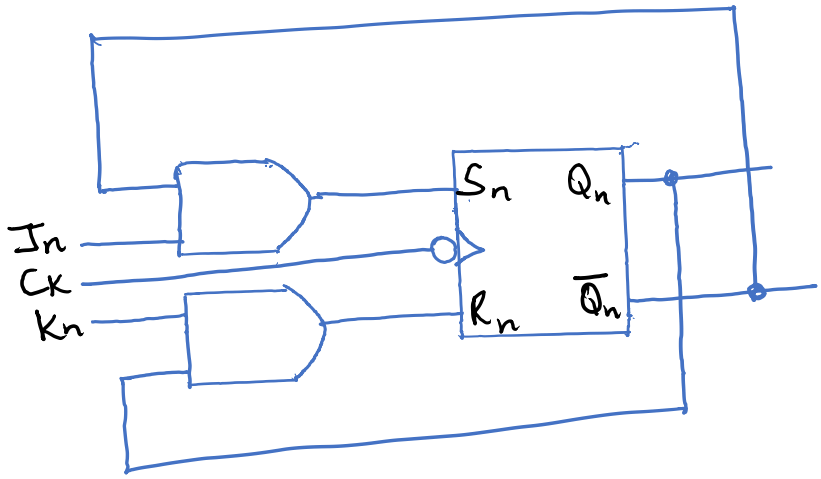
B. JK Flip Flops

- Named after Jack Kilby
- Is an improvement on the SR flip flop:

  Limitation of SR FF: Invalid condition at $S_n = 1$ and $R_n = 1$

  With JK, both inputs J_n and K_n can be at Logic 1 simultaneously.

Converting SR FF into a JK FF:



$$S_n = J_n \overline{Q}_n$$

$$R_n = K_n Q_n$$

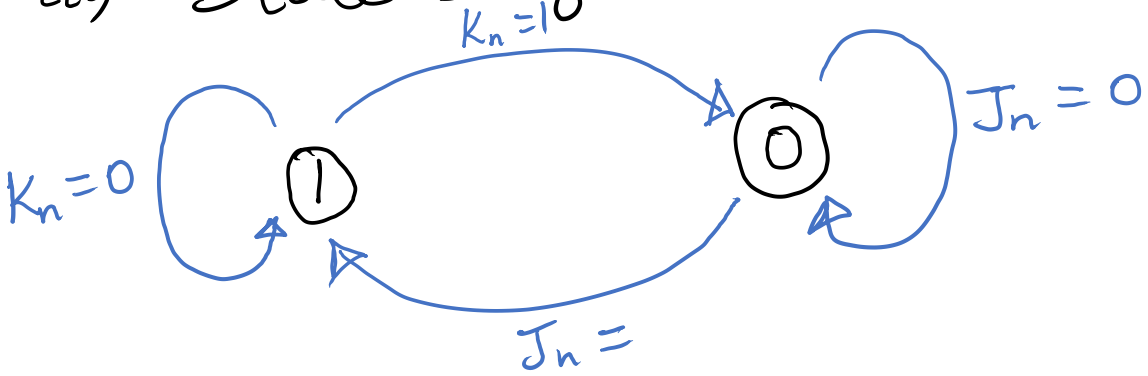
i) Characteristic Table of JK FF

Inputs J_n	Inputs K_n	NS Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

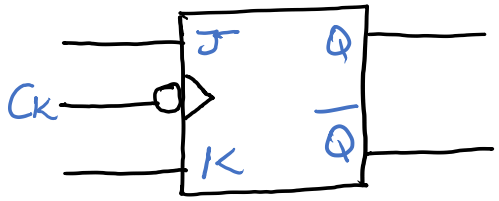
ii) Excitation Table of JK FF

PS Q_n	NS Q_{n+1}	Required Inputs J_n	K_n
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

iii) State Diagram



JK FF symbol

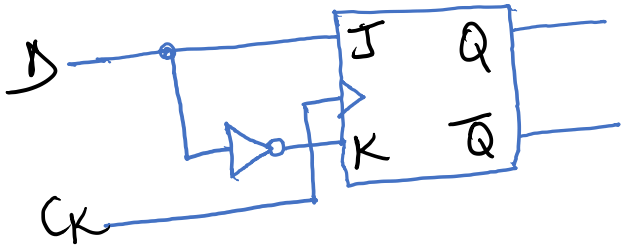


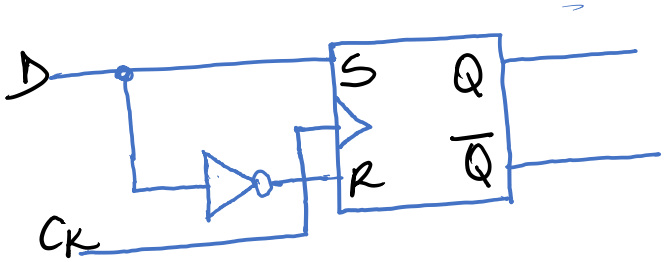
C. D (Delay) Flip Flop

- Input data appears at the output after the clock pulse
- It ensures that the invalid input combinations S=1 & R=1 for the SR FF can never occur.
- Is also called a “transparent latch’ since the output Q follows the D input when CLK=1. Hence the transfer of inputs to outputs is transparent as if the FF were not present.

Converting SR / JK FF into D FF:

- Introduce an inverter across the inputs





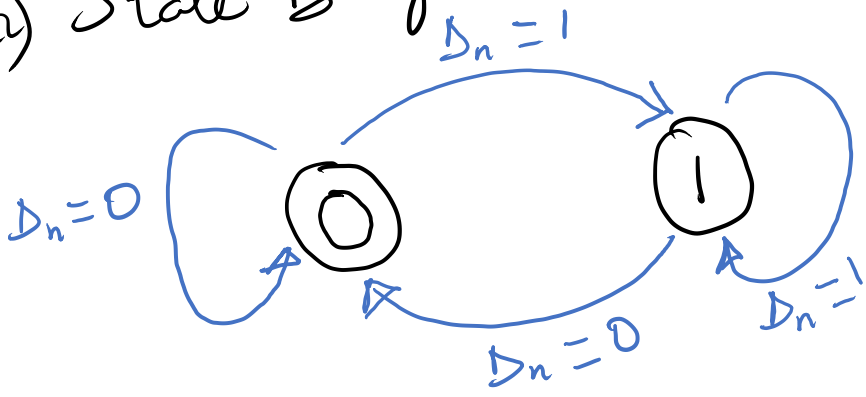
i) Characteristic Table

Inputs D_n	NS Q_{n+1}
0	0
1	1

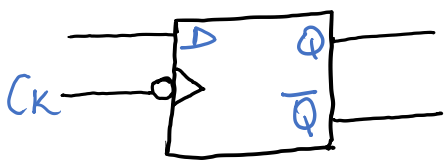
ii) Excitation Table

PS Q_n	NS Q_{n+1}	Required Input D_n
0	0	0
0	1	1
1	0	0
1	1	1

iii) State Diagram



D FF Symbol

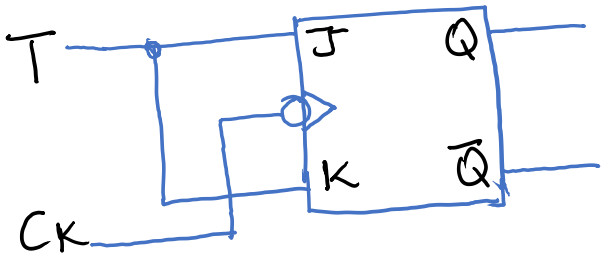


D. T (Toggle) Flip Flop

- Complements (toggles) its output when the clock input is applied with T = 1. The output remains unchanged when T = 0.

Converting JK FF into T FF

- By shorting J & K inputs to provide the T input. The output is complemented when T = 1 at the clock whilst the output remains unchanged when T = 0 at the clock.



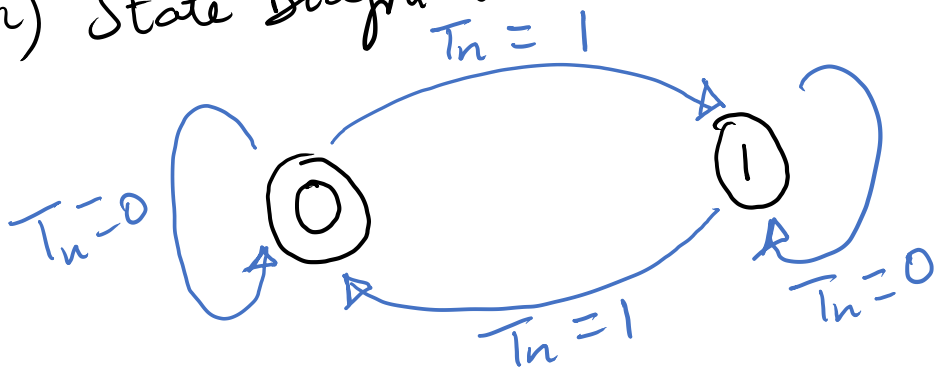
i) Characteristic Table

Input T_n	Output Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

ii) Excitation Table

PS Q_n	NS Q_{n+1}	Required Input T_n
0	0	0
0	1	1
1	0	1
1	1	0

iii) State Diagram



T FF symbol